

# SN32F700 Series

# **QUICK START**

SN32F707 SN32F706

# **SONiX 32-Bit Cortex-M0 Micro-Controller**

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#### AMENDENT HISTORY

Version	Date	Description				
1.0	2012/04/09	First version.				
1.1	2012/05/03	<ol> <li>Add CMSIS-SVD (System View Debug) section.</li> </ol>				
1.2	2012/08/08	<ol> <li>Modify CMSIS-SVD (System View Debug) section.</li> </ol>				
1.3	2013/02/27	<ol> <li>Modify refer to SN32F707 Starter kit V3.</li> </ol>				



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# 1 OVERVIEW

The purpose of this document is to make the users be familiar with SONiX SN32F700 Quick Start Development Package and the settings of Keil MDK-ARM.

# 1.1 SN32F700 QUICK START DEVELOPMENT PACKAGE

SN32F700 Quick Start Development Package includes H/W

- 1. SN32F707 Starter Kit Board
- 2. SN-LINK
- 3. SN32F700 ISP Board

#### S/W

- 1. SN32F700 CMSIS Files
- 2. SN32F700 Flash Algorithm file
- 3. SN32F700 FW Library
- 4. SN32F700 Tool Installer

## 1.2 KEIL MDK-ARM

The MDK-ARM is a complete software development environment for Cortex<sup>™</sup>-M, Cortex-R4, ARM7<sup>™</sup> and ARM9<sup>™</sup> processor-based devices. MDK-ARM is specifically designed for microcontroller applications, it is easy to learn and use, yet powerful enough for the most demanding embedded applications.

- Complete support for Cortex-M, Cortex-R4, ARM7, and ARM9 devices
- Industry-leading ARM C/C++ Compilation Toolchain
- **\square**<u> $\mu$ Vision4</u> IDE, debugger, and simulation environment
- Keil <u>RTX</u> deterministic, small footprint real-time operating system (with source code)
- TCP/IP Networking Suite offers multiple protocols and various applications
- <u>USB Device</u> and <u>USB Host</u> stacks are provided with standard driver classes
- Complete <u>GUI Library</u> for embedded systems with graphical user interfaces
- ULINK*pro* enables on-the-fly analysis of running applications and records every executed Cortex-M instruction
- Complete <u>Code Coverage</u> information about your program's execution
- Execution Profiler and Performance Analyzer enable program optimization
- Numerous example projects help you quickly become familiar with MDK-ARM's powerful, built-in features
- <u>CMSIS</u> Cortex Microcontoller Software Interface Standard compliant



MDK-ARM is available in 4 editions: MDK-Lite, MDK-Basic, MDK-Standard, and MDK-Professional. All editions provide a complete C/C++ development environment and MDK-Professional includes extensive middleware libraries. Refer to the <u>Product Selector</u> for more details.

Note: MDK-Lite (32KB) Edition is available for <u>download</u>. It does not require a serial number or license key.

Please link to <u>http://www.keil.com/arm/mdk.asp</u> to download and see more detail introduction.



# 2 SETUP

## 2.1 SN32F700 Starter-kit Board



JP46 $\rightarrow$  Mini USB connector. S1 $\rightarrow$  AC 7.5 V POWER Switch

S2→ Choose the source of VDD (LDO 3.3V or WRITER). Please switch to VDD\_WT if the WRITER is used.

J20→ Short (P0.2 and VSS) )to enter Boot Loader to ISP.

J17→ Connector for JTAG

J7 → Connector for SN-LINK/SN32F700 ISP Board



## 2.2 ICE

- 1. Please execute SN32F700 Tool Installer to install files of CMSIS and SN-LINK
- 2. Connect SN-LINK debugger and PC via USB cable

### 2.3 KEIL MDK-ARM

1. Please link to <a href="http://www.keil.com/arm/mdk.asp">http://www.keil.com/arm/mdk.asp</a> to download and install to default path (C:\ARM)

Note: The default path which FW Library provided by SONiX references is C:\ARM, if User changes the path, please modify the project settings according to the new path.

2. Open any project of SN32F700 FW Library with MRK-ARM, and then click the following button("Target Options")

🔣 E.\Working\Cortex\SN32F700_FW_LIB_CMSIS\LED toggle\SN32F70A_Demo.uvproj - 4.Vision4
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>P</u> uoject Flash <u>D</u> ebug Penjahenals <u>T</u> ools <u>S</u> VCS <u>W</u> indow <u>H</u> elp
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😵 🎬 🕮 🧼 🚉  Target 1 👘 🖍 🔒 🔁
Project 4 X 🔜 SN32F700.h 📩 maan.c 🔝 startup_SN32F700.s 🔄 SysTick.c 🛄 Utility.h 📩 Utility.c 📩 system_SN32F700.c 🛄 std
Image:
Build Output

4		
	Cortex-M/R J-LINK/J-Trace	CAP NUM SC



3. Enter "Target Options" page, click "Debug" tab, and set as the following settings, and then click "Settings" button.

💘 Options for Target 'Target 1'						
Device Target Output Listing User C/C++ A:	sm Linker Debug Utilities					
C Use <u>S</u> imulator Settings	⊡se: SN-Link Debugger     Settings     Settings					
✓ Load Application at Startup ✓ Run to main() Initialization File: … Edit	Load Application at Startup Run to main() Initialization File: Edit					
Restore Debug Session Settings Breakpoints  Toolbox Watch Windows & Performance Analyzer Memory Display	Restore Debug Session Settings Breakpoints Toolbox Watch Windows Memory Display					
CPU DLL: Parameter:       SARMCM3.DLL	Driver DLL: Parameter: SARMCM3.DLL					
Dialog DLL: Parameter: DARMCM1.DLL	Dialog DLL: Parameter: TARMCM1.DLL					
OK Cau	ncel Defaults Help					

4. Enter Setup page, KEIL shall be able to get and the status of MCU if ICE is connected correctly.

Debug Adapter	SW Device IDCODE Device Name SWDIO 0x0BB11477 ARM CoreSight SW-DP Up
Senal Number:   HW Version:	Down
Port: SW	Automatic Detection ID CODE:     Manual Configuration Device Name:
Debug Connect & Reset Options Connect: Normal	Add Delete Update IR len: Cache Options Download Options teset: Autodetect 🔽 🔽 Cache Code
Reset after Connect	Cache Memory Download to Flash



5. Please click "Utility" tab, choose SN-LINK Debugger, and then click "Settings" button.

💘 Options for Target 'Target 1'
Device Target Output Listing User C/C++ Asm Linker Debug Utilities
Configure Flash Menu Command
Use Target Driver for Flash Programming
SN-Link Debugger 💽 Settings 🔽 Update Target before Debugging
Init File: Edit
Use External Tool for Flash Programming
Command:
Arguments:
E Run Independent
OK Cancel Defaults Help

6. Please set as the following settings, and then click "Add"→ choose "SN32F700 32KB Flash"



💘 Options for Target Target 1'	×
Device Target Output Listing User C/C++ Asm Linker Debug Utilities	
SN-Link Setup	×
Debug Flash Download	
Download Function       C Erase Full Chip       ✓ Program         C Erase Sectors       ✓ Verify       Start:       0x20000000       Size:       0x2000         C Do not Erase       □ Reset and Run       □       Start:       0x20000000       Size:       0x2000	
rogramming Algorithm	Add lash Programming Algorithm 🔀
Description Device Type Device Size Address Range	
SN32F700 32KB Flash On-chip Flash 32k 00000000H - 00007FFFH	SN32F700 32KB Flash On-chip Flash 32k
Start: Size:	
Add Remove	
OK Cancel Defaults	
	Add Cancel

- Note: If "SN32F700 32KB Flash" can NOT be found, please make sure the step 2 of <u>2.3KEIL MDK-ARM</u> completes.
- 7. Please click "OK" to exit "Target Options"

### 2.4 Debug

The users can develop and debug with MDK-ARM after above settings.



SN32F700 Series

32-Bit Cortex-M0 Micro-Controller

Cortex/SN32F70	0_FW_LIB_CMSISUED toggleWN32F70A_Demo.uvproj - µVision4
File Edit View Project I	Flash Debuz Peniphenals Tools SVCS Window Help
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Project 🏾 🗖 🗙	🛄 SN32F700.h 🛃 main.c 🔝 statup_SN32F700.s 🔛 SysTick.c 🛄 Utility.h 🔛 Utility.c 🔝 system_SN32F700.c 🛄 stdi
🖃 🖳 Target 1	001 /***********************************
□	002       * COMPANY:       SONIX         003       * DATE:       2011/11         004       * AUTHOR:       SAI         005       *       IC:       SN32F700         006       *       IC:       SN32F700         007       * REVISION Date       User       Description         008       0.1       2011/11/09 SAI       1. First release         009       *       .       THE PRESENT SOFTWARE WHICH IS FOR GUIDANCE ONLY AIMS AT PROVIDING CUSTOMERS         001       *       .       .       First release         003       *       .       .       First release         004       *       .       .       First release         005       *       .       .       .         006       *       .       .       .         007       * THE PRESENT SOFTWARE WHICH IS FOR GUIDANCE ONLY AIMS AT PROVIDING CUSTOMERS       .         008       * THE PRESENT SOFTWARE WHICH IS FOR GUIDANCE ONLY AIMS AT PROVIDING CUSTOMERS       .         003       * NAMAGES WITH RESPECT TO ANY CLEAIMS ARISING FROM THE CONTENT OF SUCH SOFTWARE         104       * DAMAGES WITH RESPECT ON ANY CLEAIMS ARISING FROM THE CONTENT ON CONTAINED HEREIN         105       * In Clude "SM32F700
- <u>-</u>	031 /* DEFINITIONS*/
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Build Output	

4		
	Contex-M/R J-LINK/J-Trace	CAP NUM SC

## 2.4.1 CMSIS-SVD (System View Debug)

SONAX

SVD is the debug standard of CMSIS, and it is a useless debug tool for users.

- 1. Please make sure that you had executed SN32F700 Tool Installer to install CMSIS files
- 2. Open any project of SN32F700 FW Library with MRK-ARM, and then click the following button("Target Options")



	Control M/D LI DIV/L To	CARMINA
<u></u>		



W Options for larget Target       Device Target Output Listing User C/C++ Asm Linker Debug Utilities         ARM Cortex-M0	3. Enter "	l arget O	ptions" page	e, click "I arge	et″ tab, ar	nd click "	'" butt	on of Systen	n-Viewer file	(.Sfr) settin
Device       Target       Output       Listing       User       CAC++       Asm       Linker       Debug       Utilities         ARM Cortex-M0	VA Options f	or larget	Target I							<u> </u>
ARM Cortex-M0	Device	Target (	Output   Listin	g   User   C	/C++   As	m ∣Li	nker   D	ebug   Utilitie	s	
System: None   System: No	ABM Cort	ABM Cortex-M0								
Vial (MHz):   Dperating system:   None   System-Viewer File (Sfr):     Bead/Only Memory Areas   default off-chip   Start   Size   None:   Start   Size   Start   Size   Nonhit   ROM1:   Start   Size   Nonhit   RAM2:   Start   Size   Nonhit   RAM3:   Start   Size   Non-chip   IROM2:   IROM2: <t< td=""><td>1</td><td colspan="9">Code Generation</td></t<>	1	Code Generation								
Operating system: None   System-Viewer File (.Sfr):     Read/Only Memory Areas   default off-chip   Start   Size   None:   Start   Size   Start   Size   Start   Size   Non-chip   IROM2:   IROM2:   IROM2:   Start   Start   Start   Size   Start   Size   Non-chip   IRAM1:   Dx2000000   Dx2000000   Dx2000000   Dx2000000   Dx2000000   Start   Start <				Xtal (MHz): 12.	J					
System-Viewer File (.Sfr):     Read/Only Memory Areas   default off-chip   Start   Size   Nolnit   Start   Size   Nolnit   Start   Size   Nolnit   Start   Size   Nolnit   Size   Nolnit   Start   Size   Nolnit   Size   Start   Size   Size   Size <td>Operating</td> <td>g system:</td> <td>None</td> <td></td> <td>-</td> <td>🗌 🗌 U:</td> <td>se Cross-N</td> <td>Aodule Optimiza</td> <td>ation</td> <td></td>	Operating	g system:	None		-	🗌 🗌 U:	se Cross-N	Aodule Optimiza	ation	
Read/Only Memory Areas   default off-chip   BOM1:   BOM2:   BOM3:   On-chip   IROM1:   IROM1:   IROM2:	System-V	iewer File	(.Sfr):			🗌 🗖 U:	se MicroL	IB [	Big Endian	
Read/Only Memory Areas   default off-chip   BOM1:   BOM2:   BOM3:   On-chip   BOM1:   Dx0   Dx8000   IBOM2:										
Read/Only Memory Areas         default off-chip       Start         Start       Size         Start       Size         ROM1:       O         ROM2:       O         ROM3:       O         on-chip       IROM1:         IROM1:       0x8000         IROM2:       O         IROM1:       0x8000         IROM2:       O	·					J				
default off-chip       Start       Size       Startup         □       ROM1:       □       ○         □       ROM2:       □       ○         □       ROM3:       □       ○         □       ROM3:       □       □         □       ROM3:       □       □         □       IROM1:       0x0       0x8000       •         □       IROM1:       0x0       0x8000       •         □       IRAM1:       0x20000000       0x2000       □         □       IROM2:       □       □       IRAM2:       □	- Read/0	Dnly Memo	ory Areas			⊢Read∧	Write Men	nory Areas		
□       ROM1:       □       ○       □       RAM1:       □       □         □       ROM2:       □       ○       □       RAM2:       □       □         □       ROM3:       ○       ○       □       RAM3:       □       □         □       non-chip       ○       □       RAM3:       □       □         □       IROM1:       0×0       0×8000       ○       □       IRAM1:       0×20000000       0×2000       □         □       IROM2:       □       ○       □       IRAM2:       □       □	default	off-chip	Start	Size	Startup	default	off-chip	Start	Size	Nolnit
□       R0M2:       □       □       RAM2:       □         □       R0M3:       □       □       RAM3:       □       □         on-chip       □       RAM3:       □       □       on-chip         ✓       IROM1:       0x0       0x8000       ○       IRAM1:       0x20000000       0x2000       □         □       IROM2:       □       □       IRAM2:       □       □		ROM1:			•		BAM1:			
□       R0M3:       □       □       RAM3:       □       □         on-chip       on-chip       on-chip       □       IRAM1:       0x20000000       0x2000       □         □       IROM2:       □       □       IRAM2:       □       □		ROM2:			•		RAM2:			
on-chip       on-chip         IROM1:       0x0       0x8000       IRAM1:       0x20000000       0x2000         IROM2:       IRAM2:       IRAM2:       IRAM2:       IRAM2:       IRAM2:		ROM3:		í –	•		RAM3:			
IROM1:       0x0       0x8000 <ul> <li>IRAM1:</li> <li>0x20000000</li> <li>0x2000</li> <li>0x2000</li></ul>		on-chip	,				on-chip	,		
		IROM1:	0x0	0x8000	۲		IBAM1:	0x20000000	0x2000	
		IROM2:			•		IRAM2:			
OK Cancel Defaults Help				OK	Can	icel	De	faults		Help

4. Please assign the SN32F700.SFR which locates at C:\Keil\ARM\SFD\SONiX\SN32F700, and then click "OPEN" button.

Select a .Sfr File					? ×
查詢(]):	🚞 SN 32F700		•	(† 🖻 💣 🎟	+
我最近的文件	■]SN 32F700.SFR				
<b>1</b> 点面					
<b>会</b> 我的文件					
<b>夏</b> 夏 我的電腦					
- <b>S</b>					
網路上的芳鄰	檔名(N):	SN32F700.SFR		•	開啓(0)
	檔案類型(I):	Ini Files (*.sfr)		▼	取消
		□ 以唯讀方式開啓(R)			1.



#### 5. Click "OK"

🖔 Options fo	or Target '	'Target 1'							2	
Device	Target )	Output   Listin	ug User   C	C/C++   As	m   Li	nker   D	ebug   Utilitie:	5		
ARM Cortex-M0										
<u> X</u> tal (MHz): 12.0										
Operating	g system:	None		Use Cross-Module Optimization						
Sustem-V	'iewer File	(Sfr):			🗌 🗌 U:	🗖 Use MicroLIB 🗖 Bjg Endian				
C:\KeilV	ARM\SFD	\SONX\SN32	F700\SN32F700	).SFR						
Deedle	Darla Marca				, Deeda		4			
default	off-chip	ory Areas Start	Size	Startup	default	off-chip	ory Areas Start	Size	Nolnit	
	ROM1:					BAM1:				
	ROM2:			0		RAM2:				
	ROM3:					RAM3:				
	on-chip	<b>.</b>				on-chip				
	IROM1:	0x0	0x8000	•		IRAM1:	0x20000000	0x2000		
	IROM2:			•		IRAM2:				
			ОК	Can	cel	De	faults		Help	

#### 6. Start to debug.

E:MCU'ST32F70A\Training/SN32F700_Startkit	Package_V1.1_NewHVCMSIS Firmware Library_V1.3%N32F700_FW_LIB_CMSIS\Template\SN32F70A_Demo.u	vproj - µVision4
<u>File Edit View Project Flash D</u> ebug Per	phezals <u>T</u> ools <u>S</u> VCS <u>Window H</u> elp	
📄 🚰 📓 🦉 🐰 🛍 隆 🗠 🗠		😪 🖃 🔧
🛯 😂 🛗 🧼 🔜 🔤 Target 1		
Project 🎵	🗙 🛄 system_SN32F700.h 🛄 SN32F700.h 🔛 Utility.c 🛄 stdio.h 📩 main.c	system_SN32F700.c
□ Target 1 □ - Solution of the second se	21       #include "SN32F700.h"         22       #include "system_SN32F700.h"         23       #include "Utility.h"         24       25         26       /* DECLARATIONS         27       28         29       /* DEFINITIONS         30       31         32       /* MACROS         34       /* FUNCTIONS         36       /************************************	*/ */ */ */



7. Enter debug mode, click "View", and then select the registers which to be watched from the "System Viewer" list.

🔣 E:\\	MCU S	T32F	70 \\Trainin	g/SN321	F700_Sta	tkit_	Package_	_V1.1_J	NewHVCM	ISIS Firm	ware Library_	_V1.3\SN321	F700_FW_LIB
<u>F</u> ile	Edi	View	/ <u>P</u> roject	Fl <u>a</u> sh	Debug	Perij	pherals	<u>T</u> ools	SVCS	<u>W</u> indow	<u>H</u> elp		
	🞢 🖥	V	status Bar			2		a litë	四周		: //= // <sub>5</sub> ; (	<b>2</b>	
RST	11		Toolbars		•	E	) 🖪 🗏	= 🛵	题 - 🚺	I • 😏	- 🔜 - 🗉	📰 -	🔆 • 📃
Registe	215	E	<u>P</u> roject Win	dow									<b>д &gt;</b>
Regi	ster	3	Boo <u>k</u> s Wind	low		SystemInit();							
<b>- (</b>	Соте	{}	Functions W	7indow		8	FOOOF	88C	BL.W	Sv	stemInit	: (Ox000	00284)
	R1	$0_{\pmb{\diamond}}$	Templates <u>Y</u>	<u>W</u> indow			۱	UT_Se	et_Reg	ister(	&SN_SYS:	1->AHBCI	KEN, 16,
	R2 R3	2	Source <u>B</u> rov	vser Wind	low	iC F	2301		MOVS	r3	,#OxO1 ∽2		-
	R4	==	Build Outpu	t Wi <u>n</u> dov	,		HOIM		nov	12	,13		
	R5 R6	×	Find In File:	s Windov	,		SYSTE	M 🕨	2F700.s	Υ	system_SN3	2F700.h	 = ×
	R7 R8	⊳	<u>C</u> ommand V	Vindow			GPIO	•	ne				
	R9	Ø.	Disassembly	y Window	,		ADC		ne *****	******	*******	******	********
	R1 R1	Is	Symbo <u>l</u> Wir	vobr			WDT						
	R1:		Registers W	'indow			RTC		gure S	System	Clock wit	h Config	uration V
	R1	<u>ک</u>	Call <u>S</u> tack V	Window			TIMER	L 🕨					
	RI xPS		Watc <u>h</u> Wind	lows	•		PMU		Z_M2&	781->AH 781->AP	BCLKEN, 1 BCP1 0	$\begin{pmatrix} 6, & 1, & 1 \\ 3 & 0 \end{pmatrix}$	; //Enat //USAE
	N		<u>M</u> emory Wi	ndows	•		SSP	•				5, 57,	
	C		Serial Wind	ows	+		12C	•					
	¥		<u>A</u> nalysis Wi	indows	+		USAR?	г 🕨					
	ISF	1	Trac <u>e</u>		Þ		12S						
	Banked		System <u>V</u> ier	wer	•		FLASH	I	*****	******	*******	******	*******
l 🕂	system	-		-		11	on	- · ·	ardFau l	lt Hand	ler		

8. Take SN\_SYS0 as example, 为例, we can see the following messages in KEIL debug window.



SN SYSO

ф×

-	·							
	•							
Property	Value							
- ANBCTRL	0x00000001							
- IHRCEN	1: Enable = Enable							
- ELSEN	0: Disable = Disable							
- EHSEN	0: Disable = Disable							
EHSFREQ	0: Low = Less equal than 12MHz							
PLLCTRL	0x00000063							
- MSEL	0x03							
- PSEL	3:011 = P=6							
- FSEL	0: $F=1 = F=1$							
- PLLCLKSEL	0: IHRC = IHRC							
- PLLEN	0: Disable = Disable							
🚊 CSST	0x00000001	[						
- IHRCRDY	1: IHRC Ready = IHRC Ready							
- ELSRDY	0: ELS XTAL Not Ready = ELS XTAL Not Ready							
- EHSRDY	0: EHS XTAL Not Ready = EHS XTAL Not Ready							
- PLLRDY	0: PLL unlocked = PLL unlocked	1						
CLKCFG	0							
+ AHBCP	0							
🕂 RSTST	0x00000019							
E LVDCTRL	0	◄						
CSST [Bits 310] RO (@ 0x40060008) Offset:0x08 Clock Source Status Register								



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